IN-SITU STRIP PROCESS FOR POLYSILICON ETCHING IN DEEP SUB-MICRON TECHNOLOGY

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to a method of fabricating semiconductor structures, and more particularly, to a method of patterning a polysilicon layer in the manufacture of an integrated circuit device.

(2) Description of the Prior Art

Polysilicon pattern definition remains a significant challenge in semiconductor manufacturing. The minimum width of the polysilicon layer determines the minimum transistor length of MOS technologies. Transistor switching speed and packing density depend heavily on the ability to reliably and repeatably manufacture transistors with very narrow polysilicon gates.

Referring now to FIG. **1**, a cross-section of a partially completed prior art integrated circuit device is shown. A gate oxide layer **14** overlies a semiconductor substrate **10**. A polysilicon layer **18** overlies the gate oxide layer **14**. A hard mask layer **22** overlies the polysilicon layer **18**. Finally, a photoresist layer **26** overlies the hard mask layer **22**. Note that the photoresist layer **26** has been patterned by, for example, a photolithographic sequence of coating, exposure, and development.

Referring now to FIG. **7**, the polysilicon layer **18** is patterned using the prior art sequence that is illustrated by the process flow chart. Note, first, that the prior art process etches the pattern of the photoresist layer **26** into the hard mask layer **22** in step **30**. Second, the photoresist layer **26** is stripped away in step **34**. Third, the pattern of the hard mask layer **22** is etched into the polysilicon layer **18** in step **38**. Finally, the hard mask layer **22** is stripped away in step **42**. Note that an intervening resist strip (step **34**) necessitates the removal of the wafers from the etching chamber between the hard mask etch (step **30**) and the gate etch (step **38**).

Referring now to FIG. **2** and to FIG. **7**, step **30**, the photoresist layer **26** may be trimmed. This trimming step is performed to reduce the width of the photoresist layer **26** to a dimension that is smaller than the capability of the photolithographic exposure equipment. This trimming etch is performed in the plasma dry etch chamber and reduces the width of the patterned photoresist layer **26** to a dimension that will enable the final patterned polysilicon layer **18** to meet the critical dimension (CD) specifications for the manufacturing process.

Referring now to FIG. **3** and to FIG. **7**, step **30**, the pattern of the photoresist layer **26** is etched into the hard mask layer **22**. This etching step is again performed in the plasma dry etch chamber.

Referring now to FIG. **4** and to FIG. **7**, step **34**, the photoresist layer **26** is stripped away. This photoresist layer **26** must be removed to improve the selectivity of the plasma dry etch process. Because the gate oxide layer **14** of the deep sub-micron process is very thin, the subsequent polysilicon etching step must have a high selectivity to the gate oxide. Removing the photoresist layer **26** prior to the polysilicon etch step **38** improves this selectivity. This is the reason that the hard mask layer **22** is used.

Of particular importance to the present invention is the fact that the semiconductor wafers must be removed from the plasma dry etch chamber during photoresist stripping. A separate photoresist stripping chamber is typically used to strip away this remaining photoresist. Following the photoresist strip, the wafers are then returned to the plasma dry etch chamber for the gate or polysilicon layer **18** etch step **38**. This polysilicon layer **18** is thereby etched in a photoresist free process that is herein called an ex-situ process.

The additional wafer handling and process equipment required to remove the photoresist layer **26** increases the cycle time and the processing cost. In addition, the wafers are open to increased contamination due to the handling and the additional processing chamber. The additional processing chamber also makes controlling processing parameters more difficult. Finally, additional inspections and CD measurement steps may be added to insure that the additional handling and process set-ups are within specification. This also adds to the processing cost and cycle time.

Referring now to FIG. **5** and to FIG. **7**, step **38**, the pattern of the hard mask layer **22** is etched into the polysilicon layer **18**. This step is performed in the plasma dry etch chamber after the photoresist strip step **34**.

Referring finally to FIG. **6** and to FIG. **7**, step **42**, the hard mask layer is stripped away to complete the patterning of the polysilicon layer **18**. The wafers are removed from the plasma dry etch chamber for this processing step **42**. The hard mask stripping may comprise a wet etch process.

Several prior art approaches disclose methods to pattern polysilicon in the manufacture of an integrated circuit device. U.S. Pat. No. 5,767,018 to Bell teaches a method to etch a polysilicon pattern where an anti-reflective coating (ARC) is used. Pitting problems are eliminated. In one embodiment, a passivation layer is formed on the sidewalls of the patterned ARC layer prior to polysilicon etching. In a second embodiment, the passivation layer is formed on the ARC layer sidewalls during the polysilicon etch. U.S. Pat. No. 6,037,266 to Tao et al discloses a method to etch a polysilicon pattern. A bottom anti-reflective coating (BARC) is used. The BARC layer and an oxide layer are etched to form a pattern over the polysilicon layer. The BARC layer is then stripped away using a biased O_2 plasma. The polysilicon layer is then etched using the oxide layer as a hard mask. U.S. Pat. No. 5,346,586 to Keller teaches a method to etch a polysilicon pattern. A silicide layer is used overlying the polysilicon layer. An oxide layer overlies the silicide layer. The oxide layer is patterned using a photoresist layer. The photoresist layer is then removed using an ozone plasma strip. The silicide layer is etched. Finally, the polysilicon layer is etched. U.S. Pat. No. 5,885,902 to Blasingame et al discloses a method to etch an anti-reflective coating (ARC) layer using an inert gaseous plasma containing helium, nitrogen, or a mixture thereof.

SUMMARY OF THE INVENTION

A principal object of the present invention is to provide an effective and very manufacturable method of patterning a polysilicon layer in the manufacture of an integrated circuit device.

A further object of the present invention is to provide a method to pattern the polysilicon layer that reduces process cycle time in the processing sequence.

Another further object of the present invention is to provide a method to pattern the polysilicon layer that reduces wafer handling.

A yet further object of the present invention is to provide a method to pattern the polysilicon layer by stripping away the photoresist layer in-situ to the polysilicon dry plasma etch chamber.

A still further object of the present invention is to provide a method to eliminate photoresist polymer residue from the polysilicon dry etch chamber.

In accordance with the objects of this invention, a new method of patterning the polysilicon layer in the manufacture of an integrated circuit device has been achieved. A polysilicon layer is provided overlying a semiconductor substrate. The polysilicon layer may overlie a gate oxide layer and would thereby comprise the polysilicon gate for MOS devices. A hard mask layer is provided overlying the polysilicon layer. A resist layer is provided overlying the hard mask layer. The resist layer is patterned to form a resist mask the exposes a part of the hard mask layer. The polysilicon layer is patterned in a plasma dry etching chamber. First, the resist layer is optionally trimmed by etching. Second, the hard mask layer is etched where exposed by the resist mask to form a hard mask that exposes a part of the polysilicon layer. Third, the resist mask is stripped away. Fourth, polymer residue from the resist mask is cleaned away using a chemistry containing CF_4 gas. Fifth, the polysilicon layer is etched where exposed by the hard mask. After the polysilicon layer is so patterned in the dry plasma etch chamber, the hard mask layer is stripped away to complete the patterning of the polysilicon layer in the manufacture of the integrated circuit device.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

FIGS. **1** through **6** illustrate in cross-section a partially completed prior art integrated circuit device.

FIG. **7** illustrates the process flow sequence for the prior art polysilicon patterning method.

FIG. **8** illustrates the process flow sequence for the preferred embodiment of the method of the present invention.

FIGS. **9** through **12** illustrate in cross-section the preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The embodiment discloses the application of the present invention to the patterning of the polysilicon layer in the manufacture of an integrated circuit device. It should be clear to those experienced in the art that the present invention can be applied and extended without deviating from the scope of the present invention.

Referring now particularly to FIG. **8**, a process flow sequence for the preferred embodiment of the present invention is shown. This process flow is of particular importance to the present invention. In the preferred process flow, the resist trim etch, hard mask etch, resist strip, and gate etch are combined into a single process step **50** within a dry plasma etch chamber. The novel method allows these processing components to be conducted using a continuous dry plasma etching recipe through the sequential introduction of gases and control of parameters. The cost, time consumption, and contamination that are introduced by the excessive wafer handling of the prior art process are thereby eliminated. After the polysilicon layer, herein called the gate, is etched, the wafers may be removed from the dry plasma etch chamber. The hard mask layer is then stripped in step **54**.

As in the prior art process, the resist trim step is optional to the method of the invention. The resist trim step may be used to reduce the line width of the photoresist layer beyond the capability limits of the photolithographic equipment.

Of particular importance to the process flow is the inclusion within the etching step **50** of a polymer clean step. After the resist layer is stripped away, residual organic polymer from the resist material may be present in the chamber and on the sidewalls of the hard mask. A polymer cleaning is therefore an essential aspect of the present invention. The organic polymer is removed using a cleaning chemistry containing CF_4 gas. The chamber and the integrated circuit device is thereby cleaned of residual organic polymer material prior to the critical polysilicon gate etch.

Referring now to FIG. **9**, a cross-section of the partially completed device of the present invention method is shown. A semiconductor substrate **60** is provided. The semiconductor substrate preferably comprises monocrystalline silicon. A gate oxide layer **64** is provided overlying the semiconductor substrate **60**. The gate oxide layer **64** is very thin in a deep sub-micron MOS process. For example, the gate oxide layer **64** is formed by conventional means to about 20 Angstroms.

A polysilicon layer **68** is provided overlying the gate oxide layer **64**. The polysilicon layer **68** may be doped or undoped and is formed by conventional means. As an example, the polysilicon of the preferred embodiment is undoped and has a thickness of between about 1,500 Angstroms and 2,500 Angstroms.

A hard mask layer **72** is provided overlying the polysilicon layer **68**. The hard mask layer **72** will subsequently be patterned to form a hard mask overlying the polysilicon layer **68** for the polysilicon etch step. The hard mask layer **72** preferably comprises silicon oxynitride with a thickness of between about 300 Angstroms and 500 Angstroms. Silicon dioxide could be used as the hard mask layer **72** in the present invention.

A silicon dioxide layer **76** is provided overlying the hard mask layer **72**. The silicon dioxide layer **76** is used as a buffer layer to gain etching selectivity during the polysilicon etching. The silicon dioxide layer **76** is optional to the present invention.

A resist layer **80** is provided overlying the silicon dioxide layer **76**. The resist layer **80** preferably comprises a conventional photoresist material that has been applied, exposed and developed to form a pattern. The resist layer **80** thereby contains the pattern that will be transferred, first, to the hard mask layer **72** and, second, to the polysilicon layer **68**. As an example, the preferred resist layer **80** comprises a deep ultra-violet (DUV) photoresist, such as ShinEtsu 233DT. The photoresist material is spin coated overlying the wafer to a thickness of between about 3,500 Angstroms and 5,000 Angstroms. Following bake, the resist layer has a thickness of between about 3,000 Angstroms and 4,700 Angstroms. The resist layer **80** is patterned, for example, to a minimum line with critical dimension (CD) of between about 0.151 microns and 0.169 microns.

Referring now to FIG. **10**, several important features of the present invention are presented. The semiconductor wafers are loaded into the dry etching chamber as outlined in the process flow step **50**. In the preferred process example, the dry plasma etching chamber comprises an Applied Materials DPS-POLY system. The overall dry plasma etching recipe sequence, shown as step **50** of FIG. **8**, comprises a series of recipe steps. Each recipe step completes a step in the process of transferring the resist layer pattern into the polysilicon layer.

The first recipe step comprises the trim etch. As in the prior art process, the trimming step is not considered an essential aspect of the method of the present invention. In the trimming etch, the resist layer **80** is etched to reduce the line widths of the resist layer **80**. In the example process, the minimum pre-trim resist layer **80** width is between about